In the Claims:

No amendments to the claims are presented

1. (Previously Presented) A frame synchronizing device for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, the device comprising:

a serial input parallel output shift register for receiving said serial bit stream and outputting said frames in a consecutive order, said shift register including a serial input portion and a parallel output portion and having at least as many stages as the number of bits of a frame,

first clock circuitry that generates first clock pulses, separated by a first time period, for clocking the serial input portion of the shift register;

second clock circuitry that generates second clock pulses for clocking the parallel output portion of the shift register, the second clock circuitry generating the second clock pulses responsive to the first clock pulses, and

control circuitry for detecting whether or not a frameheader is present at the output of said parallel output portion and, if not, controlling said shift register so that the clocking of the parallel output portion is delayed by at least the first time period, the control circuitry delaying the clocking of the parallel output portion by preventing one of the first clock pulses from reaching the second clock circuitry.

2. (Previously Presented) The device according to claim 1, wherein said control circuitry is adapted so that the preventing of one of the first clock pulses from reaching the second clock circuitry is repeated until synchronization is reached.

3. (Previously Presented) The device according to claim 1, wherein the frames have a fixed length.

4. (Original) The device according to claim 3, wherein the frames are bytes.

5. (Previously Presented) The device according to claim 1, wherein the control circuitry is adapted to control said second clock circuitry so that said second clock pulses are delayed by at least the first time period which is needed for shifting a bit in said serial input portion from a stage to a next stage.

6. (Previously Presented) The device according to claim 5, wherein each frame includes N bits, and the second clock circuitry converts said first clock pulses into said second clock pulses, the second clock pulses separated by a second time period that is N times longer than the first time period of said first clock pulses, said control circuitry is adapted to control said second clock circuitry so that said second clock pulses are delayed by at least the first time period of said first clock pulses.

7. (Previously Presented) The device according to claim 5, wherein said control circuitry is adapted to supply a control signal to said second clock circuitry to prevent the one of the first clock pulses from reaching the second clock circuitry, and said second clock circuitry is adapted so that the one of the first clock pulses is blocked by said control signal for at least the first time period which is needed for shifting a bit in said serial input portion of said shift register from a stage to a next stage.

8. (Previously Presented) A frame synchronizing method for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, the method comprising the steps of:

inputting said serial bit stream into a serial input portion of a serial input parallel output shift register having at least as many stages as the number of bits of a frame,

generating first clock pulses, by first clock circuitry, for clocking the serial portion of the shift registers, the first clock pluses separated by a first time period

generating second clock pulses, by second clock circuitry, for clocking a parallel output portion of the shift register, the second clock pulses derived from the first clock pulses,

outputting said frames in a consecutive order from the parallel output portion of said shift register,

detecting whether or not a frameheader is present in the output of said parallel output portion, and,

if not, delaying the generation of the second clock pulses by at least the first time period by preventing one of the first clock pulses from reaching the second clock circuitry.

9. (Previously Presented) The method according to claim 8, wherein the preventing of one of the first clock pulses from reaching the second clock circuitry is repeated several times until synchronization is reached.

10. (Previously Presented) The method according to claim 8, wherein the frames have a fixed length.

11. (Original) The method according to claim 10, wherein the frames are bytes.

12. (Previously Presented) The method according to claim 8, the second clock pulses are delayed by at least the first time period which is needed for shifting a bit in said serial input portion from a stage to a next stage.

13. (Previously Presented) The method according to claim 12, comprising the further steps of:

converting said first clock pulses into said second clock pulses, the second clock pulses separated by a second time period that is N times longer than the first time period of said first clock pulses, wherein each frame includes N bits, and said second clock pulses are delayed by at least the first time period of said first clock pulses.

14. (Previously Presented) The method according to claim 12, further comprising generating a control signal if a frameheader is not detected in the output of said parallel output portion of said shift register, and blocking the generation of said

second clock pulses by said control signal for at least the first time period which is needed for shifting a bit in said serial input portion of said shift register from a stage to a next stage.

15. (Previously presented) A digital data transmission systems like SONET/SDH or Gigabit Ethernet comprising a device as claimed in claim 1 where serial data are transported over a single channel and, at the receiving side, is converted into parallel data for further processing.